PCI Express® in Automotive Infotainment and ADAS Processors

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Outline

- **Automotive PCI Express® Use Cases**
- **Automotive SoC PCI Express Architecture**
- **PCI Express Functional Safety**
- **PCI Express Validation and Documentation**

Automotive PCI Express Use Cases

Automotive PCIe® Use Cases

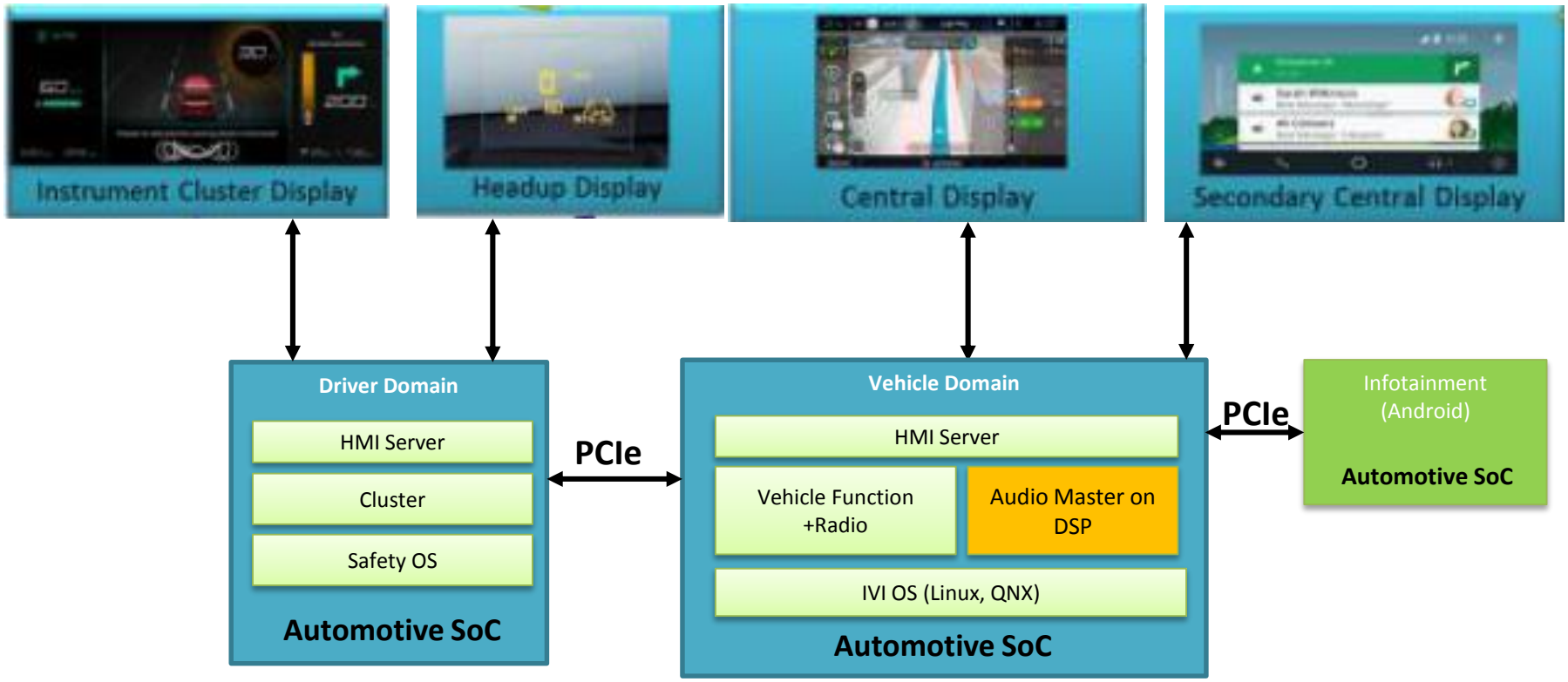
- **Inter-processor communications**
  - Main processor to specialized processor
    - Ex. GP Processor to Radio/Audio/Auto-connectivity processor
  - Homogenous multi-processor scalable architectures
    - Ex. Distributed processing of Camera/Video/Graphics data
  - Redundant fail-safe processor architecture

Automotive PCIe Use Cases

- **Peripheral communications**
  - SSD
  - LTE Modem
  - Wi-Fi / Bluetooth
  - V2X Vehicle-to-Everything (IEEE 802.11p)
    - Vehicle
    - Pedestrian / Cyclist
    - Home
    - Infrastructure
    - Etc.

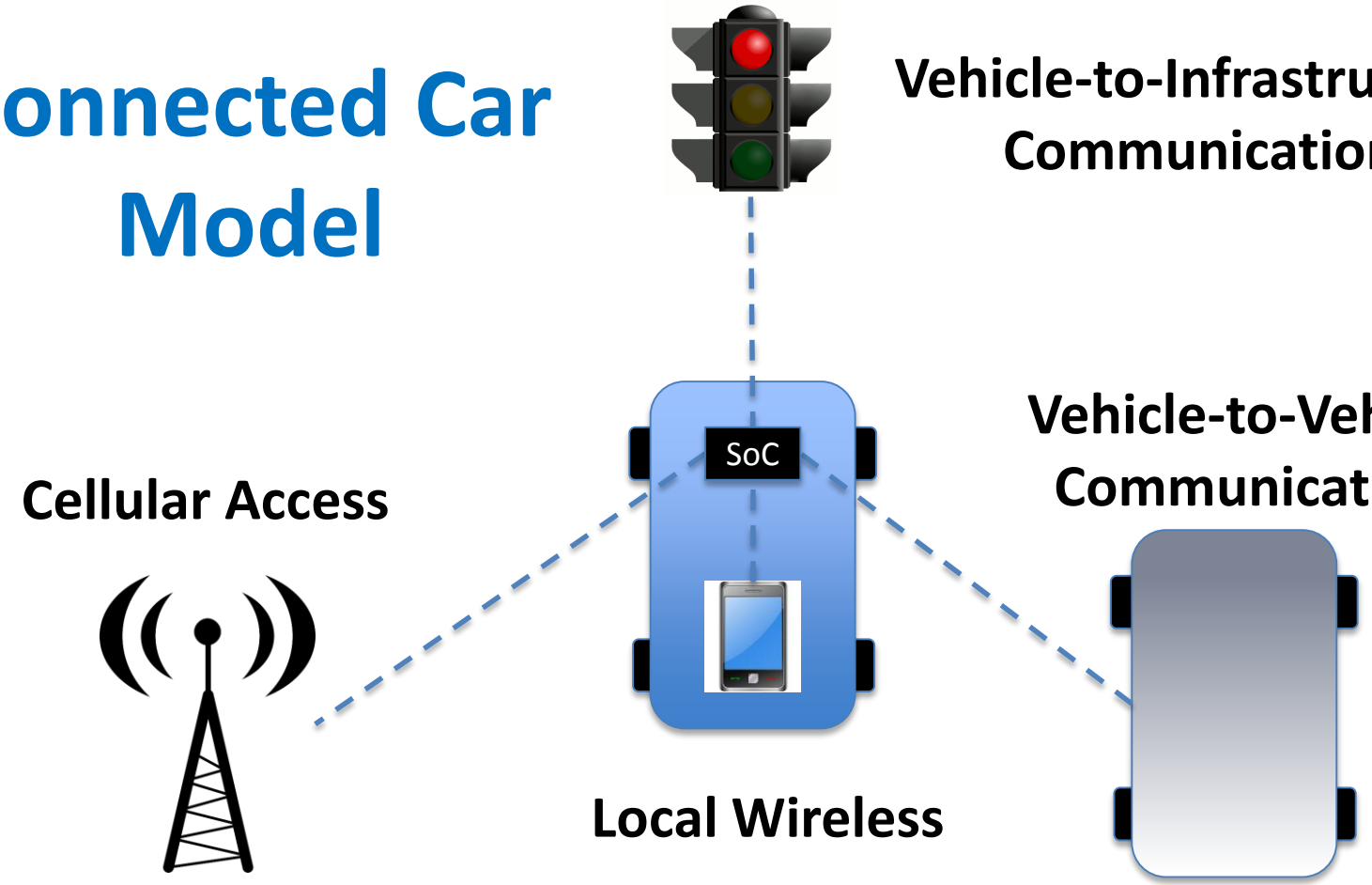
Example: Infotainment

- **Scalable Multi-Display Infotainment**
  - PCIe® provides Inter-processor Communication

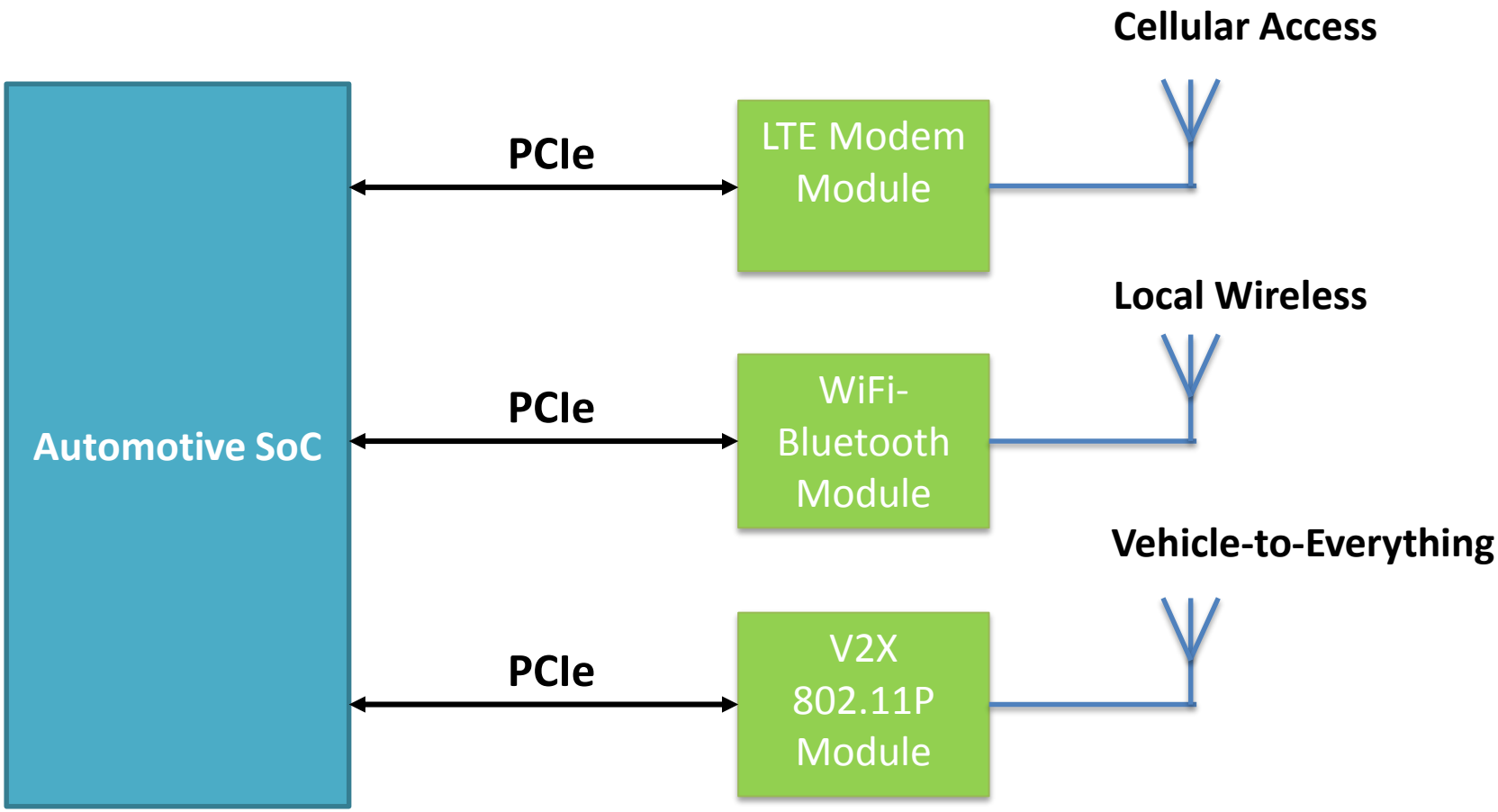


Example: Telematics (1/2)

Connected Car Model

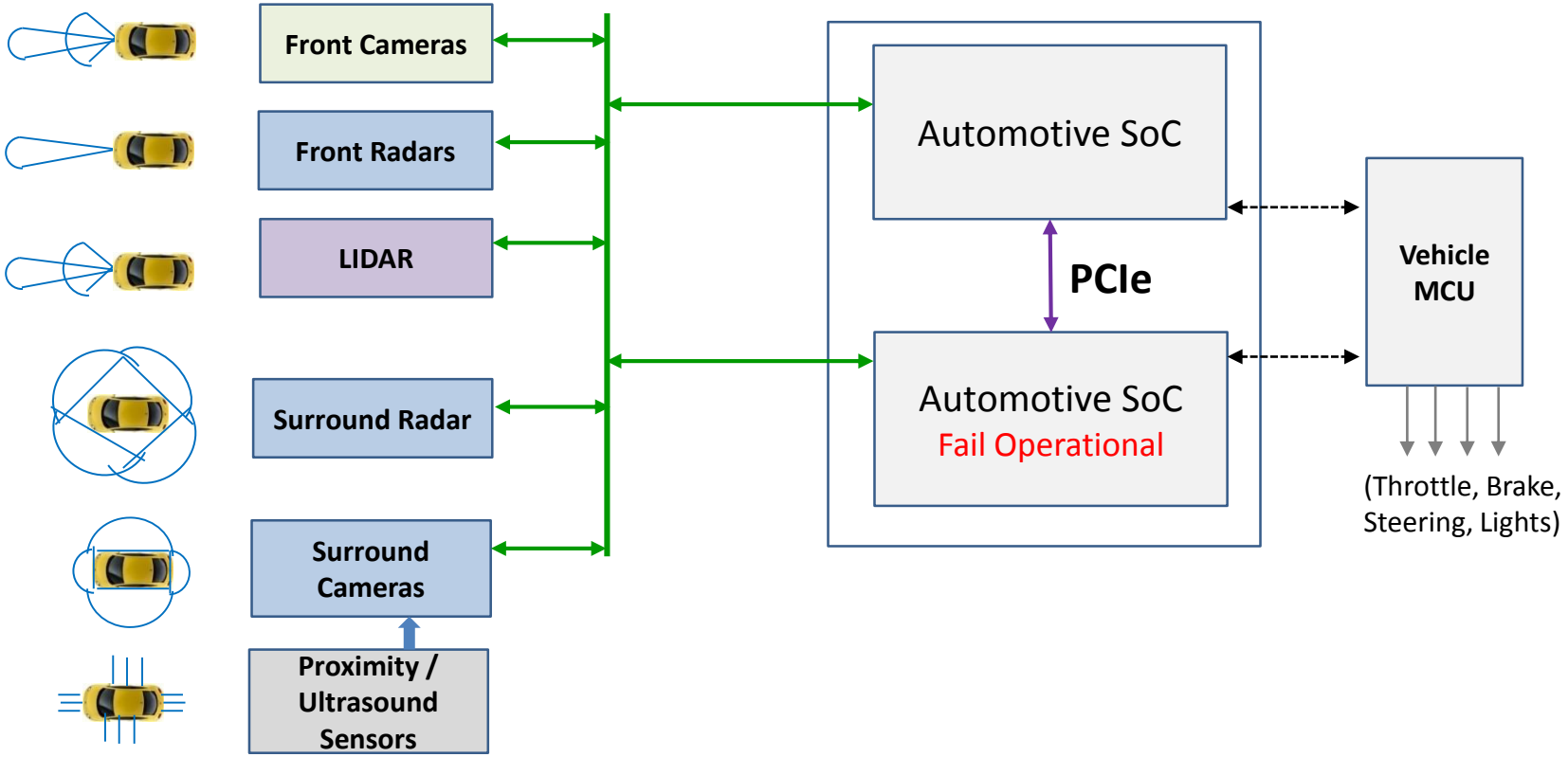


Example: Telematics (2/2)



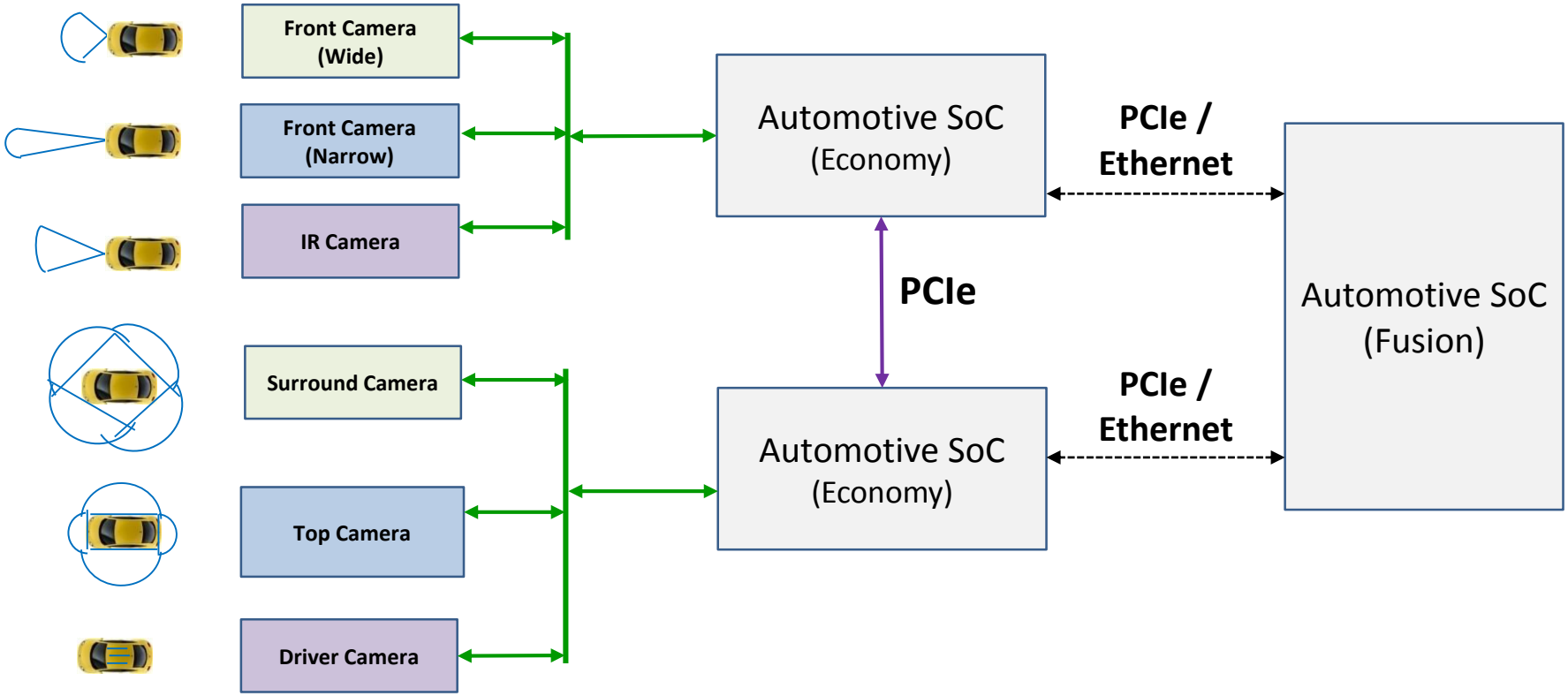
Example: ADAS

- **Redundant Fail-Operational Processor attached via PCIe**



Example: ADAS

- **Scalable ADAS features via PCIe**
  - Scalable system architecture to support both basic and advance ADAS features
  - PCIe provides Load Balancing between SoCs

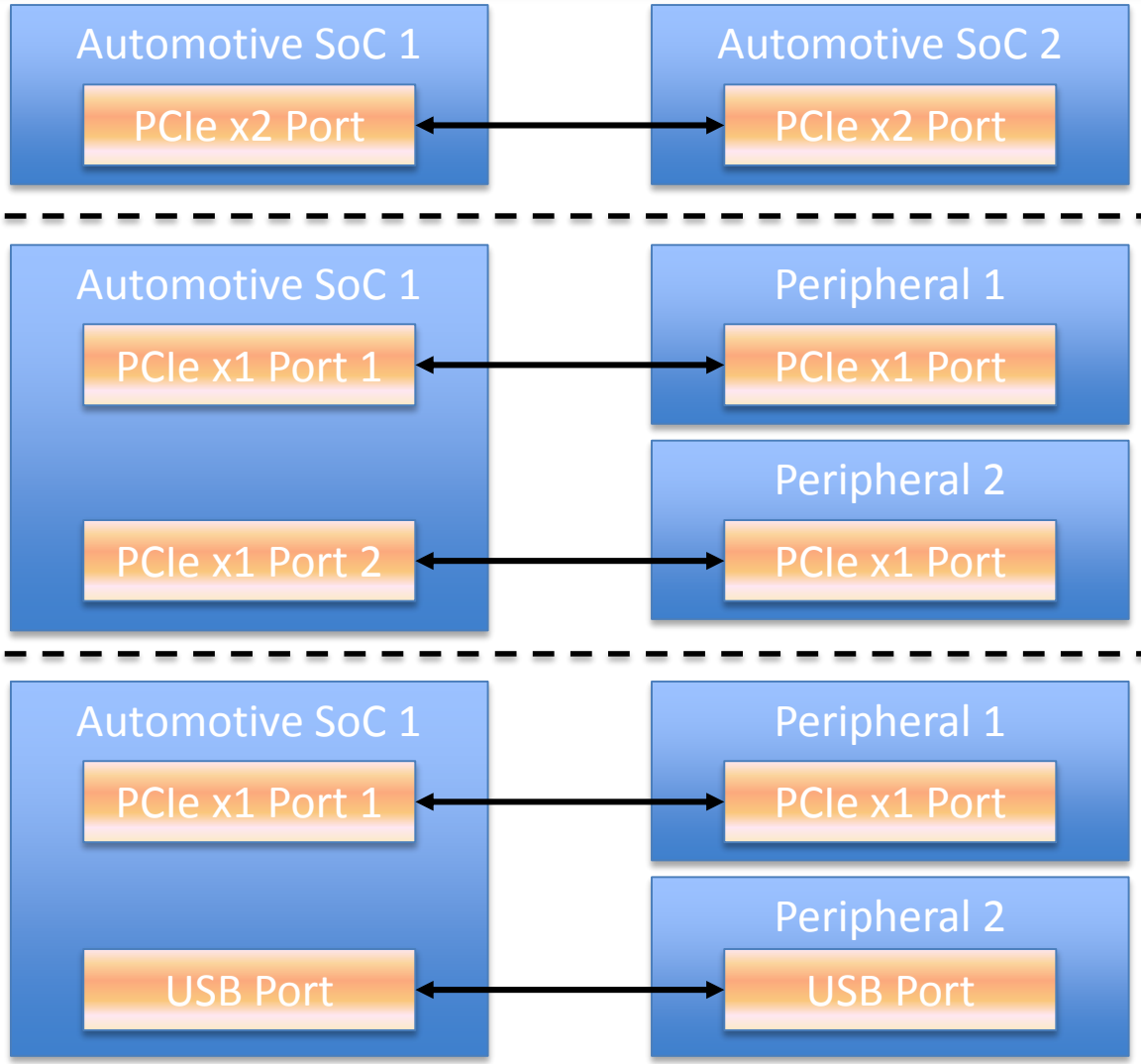


Automotive SoC PCI Express Architecture

Dual-Mode Operation (RC or EP)

- **Automotive PCIe IP is generally integrated to support both Root Complex and End Point Operation**
- **Benefit**
  - Supports diverse use cases shown in previous slides
- **Challenges**
  - REFCLK
  - Reset
  - Validation

SERDES Sharing: Motivation



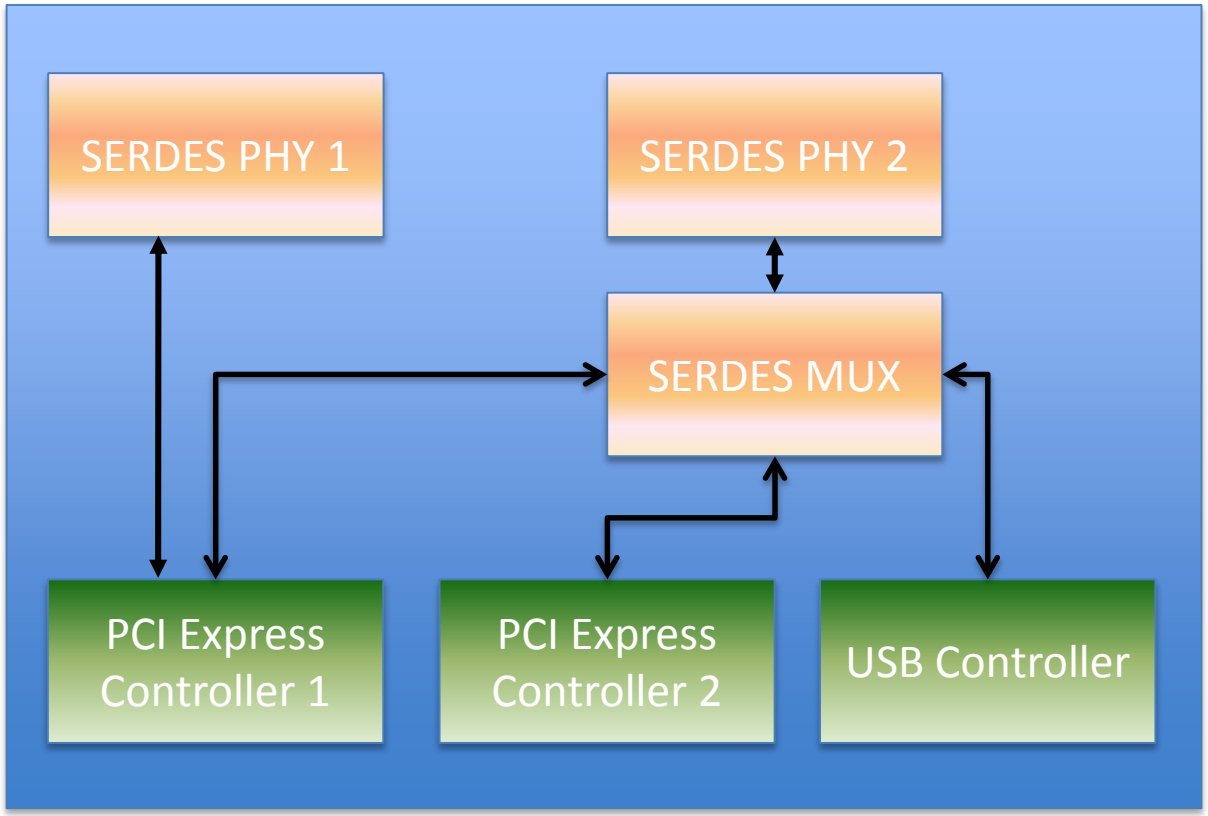
Use Case 1:
High-bandwidth Processor Comms

Use Case 2:
Dual PCIe Peripherals

Use Case 3:
Mixed PCIe and USB Peripherals

SERDES Sharing: Architecture

- **SERDES Sharing allows support for all three Use Cases by a single SoC Architecture**



Configuration 1

PCIe Port 1 Lane 0
PCIe Port 1 Lane 1

Configuration 2

PCIe Port 1 Lane 0
PCIe Port 2 Lane 0

Configuration 3

PCIe Port 1 Lane 0
USB 3.x Port

SERDES Sharing: Benefits

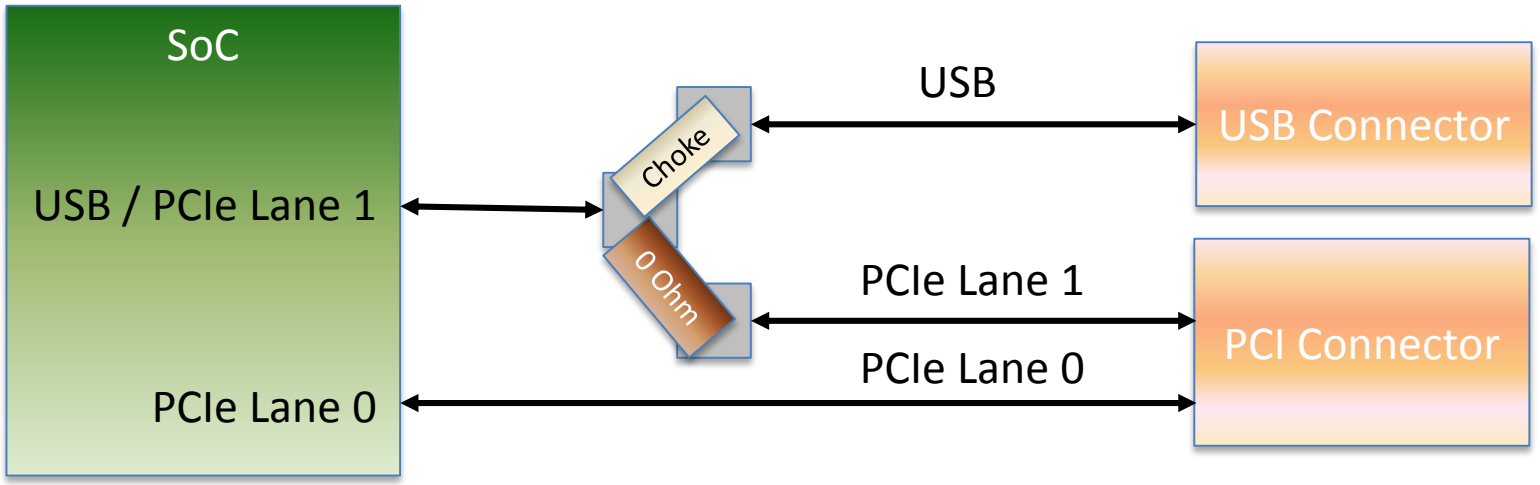
- **Supports diverse system use cases with a single Processor design**
  - Infotainment, ADAS, Industrial, Catalog
- **Reduces number of required SERDES PHYs and pins**
  - Previous example reduces PHY count from 4 to 2
  - Cuts number of required SERDES pins in half
  - Cuts SERDES die area in half
- **Allows tradeoff between number of ports and lanes/port**
  - 1 port with many lanes
  - Many ports with one lane each

SERDES Sharing: Challenges

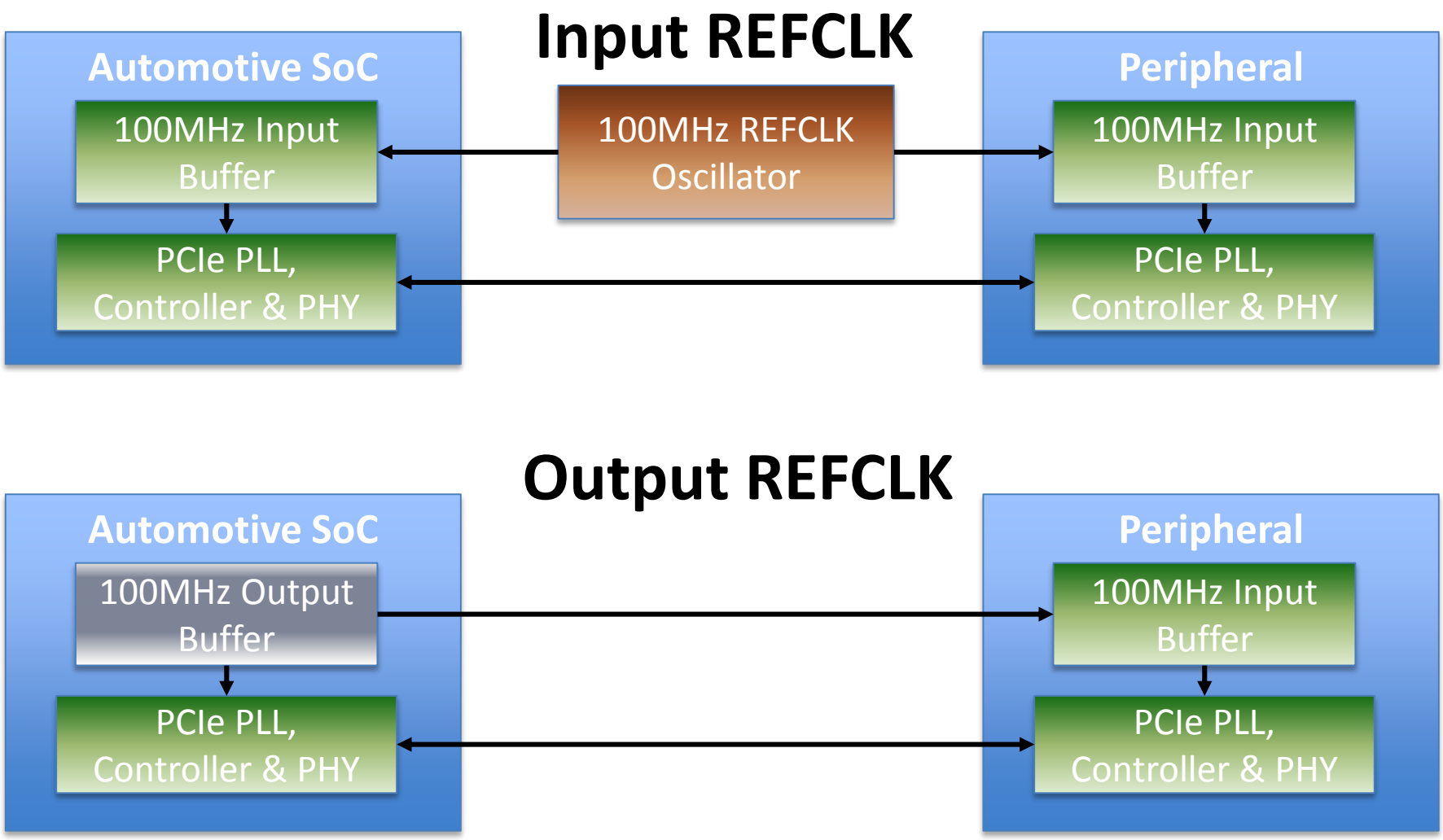
- **PHYs must be programmable to support multiple SERDES standards**
  - Software must comprehend complexity
  - PHYs must support all standard-specific signaling (LFPS, BEACON, etc.)
- **SERDES standards have different target termination impedance**
  - PCI Express = 100 Ohm vs. USB = 90 Ohm
  - PHYs should have programmable termination impedance
  - If not, PHY impedance trimming must compromise on a common value

SERDES Sharing: Challenges

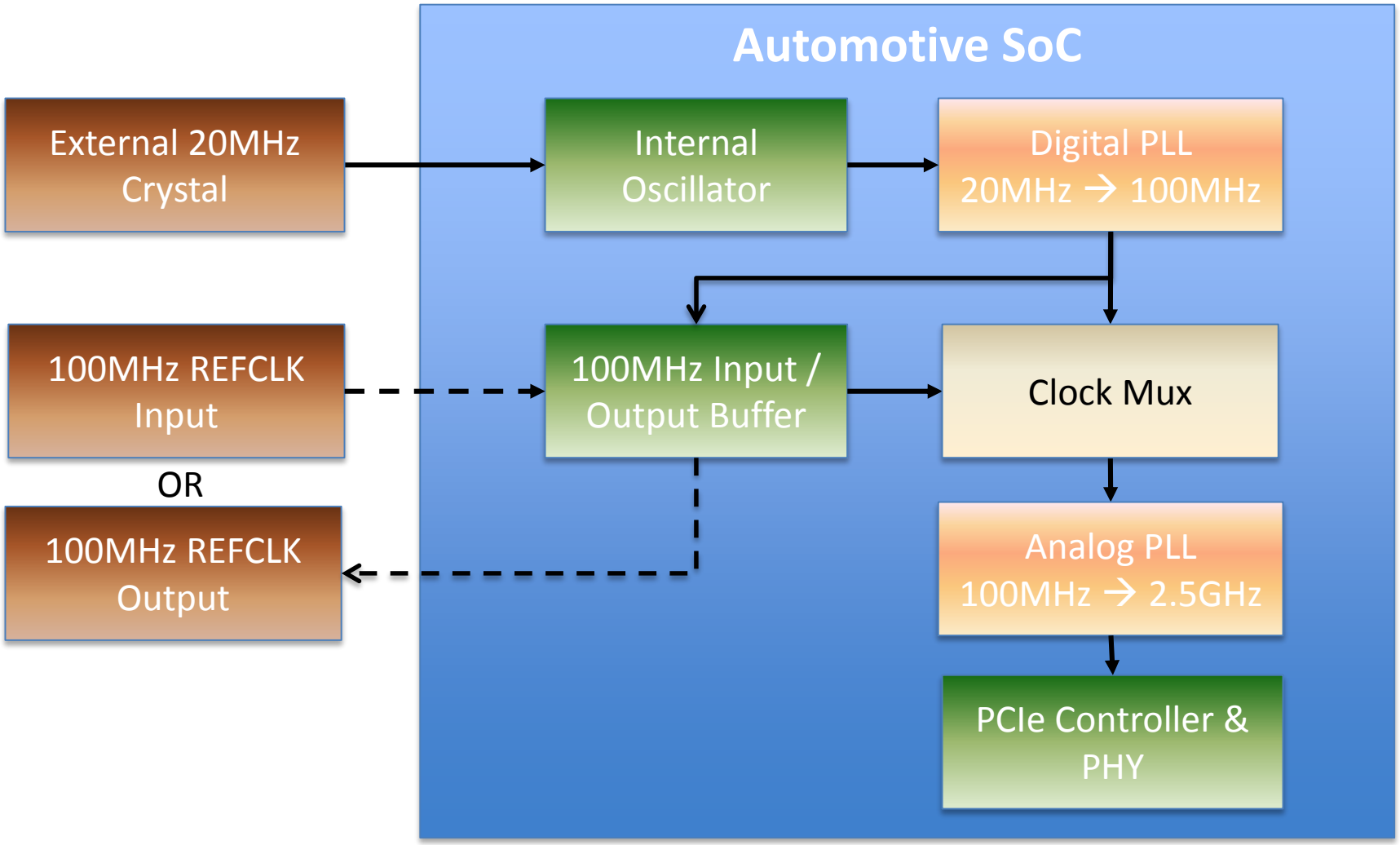
- **Evaluation boards must use PCB-level muxing**
  - Can result in non-optimal and or non-matched routes
  - Can introduce extra passive components that affect signal integrity (0-ohm resistors)
  - Not an issue for most customer production systems



REFCLK IO: System View



REFCLK IO: Architecture



REFCLK IO: Benefits

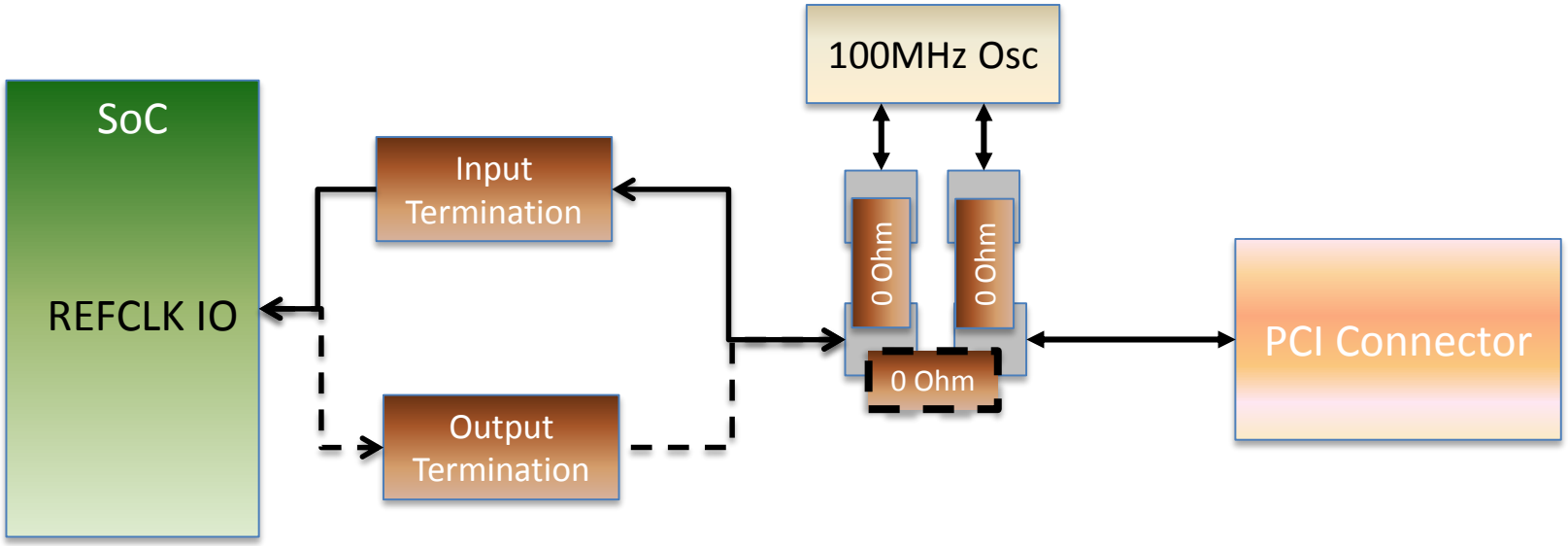
- **Output REFCLK**
  - Eliminates REFCLK oscillator from System BOM
  - Facilitates Root Complex operation in Common REFCLK system
  - Facilitates Separate REFCLK implementation without PCB-level 100MHz clock routing
- **Input REFCLK**
  - Fallback to high-quality external oscillator
  - Interop with other components or systems that only supply REFCLK

REFCLK IO: Challenges

- **Generating REFCLK from an internal PLL**
  - Requires advanced (large die area) PLLs to meet PCIe jitter requirements
- **BIDI Buffer and internal multiplexing requirements**
- **Sharing of REFCLK between multiple ports**
  - Can require multiple REFCLK IO buffers
  - Forces same SSC choice on all ports

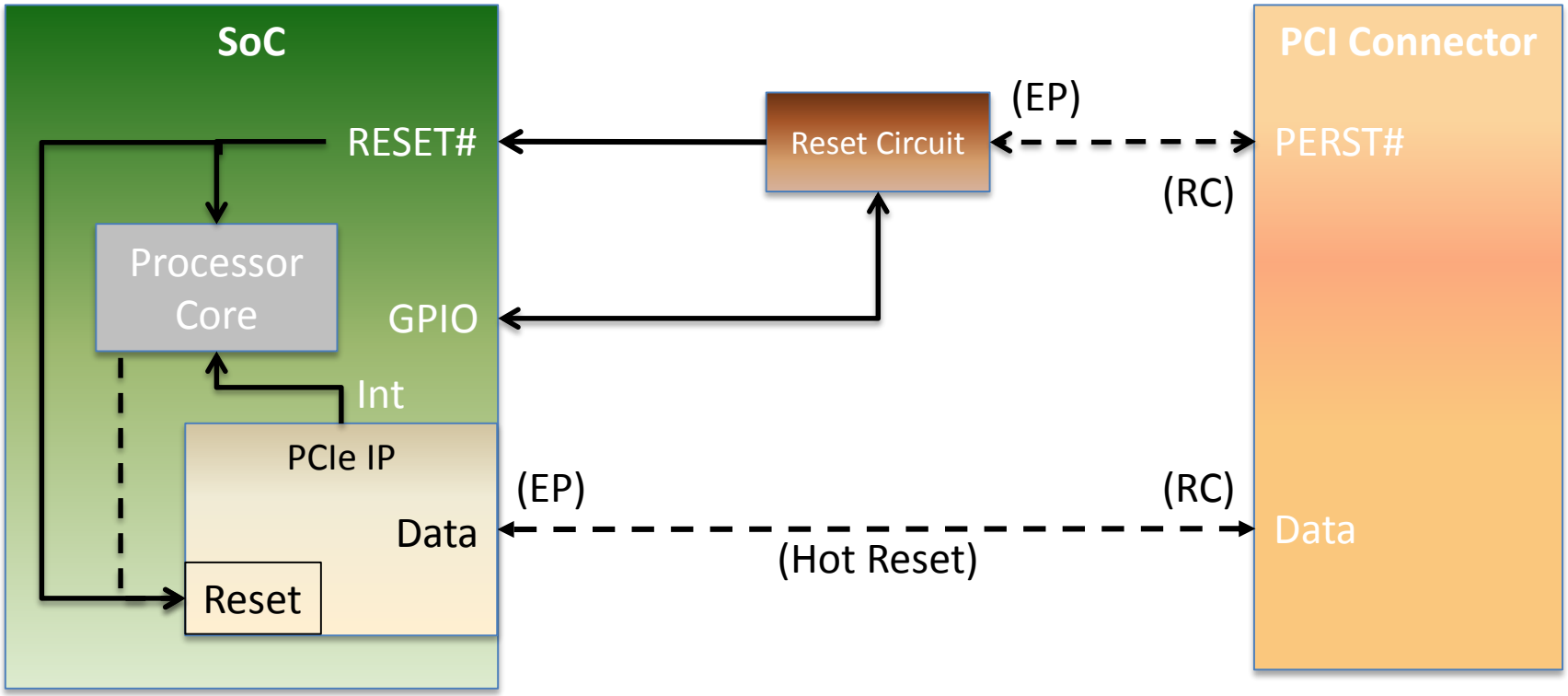
REFCLK IO: PCB

- **Evaluation board must support both Internal/External options via a layout and component population scheme**
  - Different REFCLK Termination population requirements
  - Population options to bypass external oscillator



Reset: Implementation

- **PCIe IP Reset vs SoC Reset**

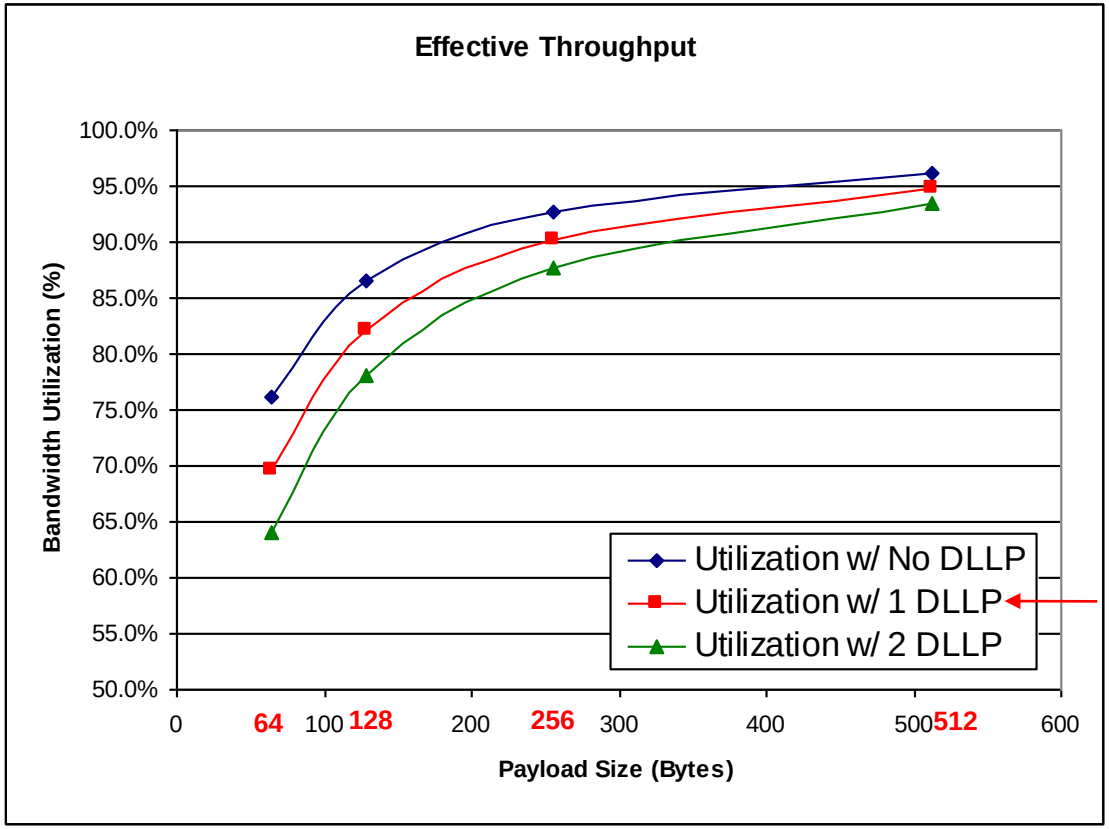


Payload Size: Implementation

- **Packet payload size has trade-offs in performance vs silicon area**
- **Outbound payloads has SoC dependencies**
  - Limited by Master IPs and processor interconnect
- **Inbound payloads**
  - Larger payloads require increase in buffer sizes
- **Common Automotive SoC implementation**
  - Ex. SoC DMA/interconnect only supports 64B transactions
    - 64B max outbound payloads
    - 256B max inbound payloads, internally split into 64B chunks

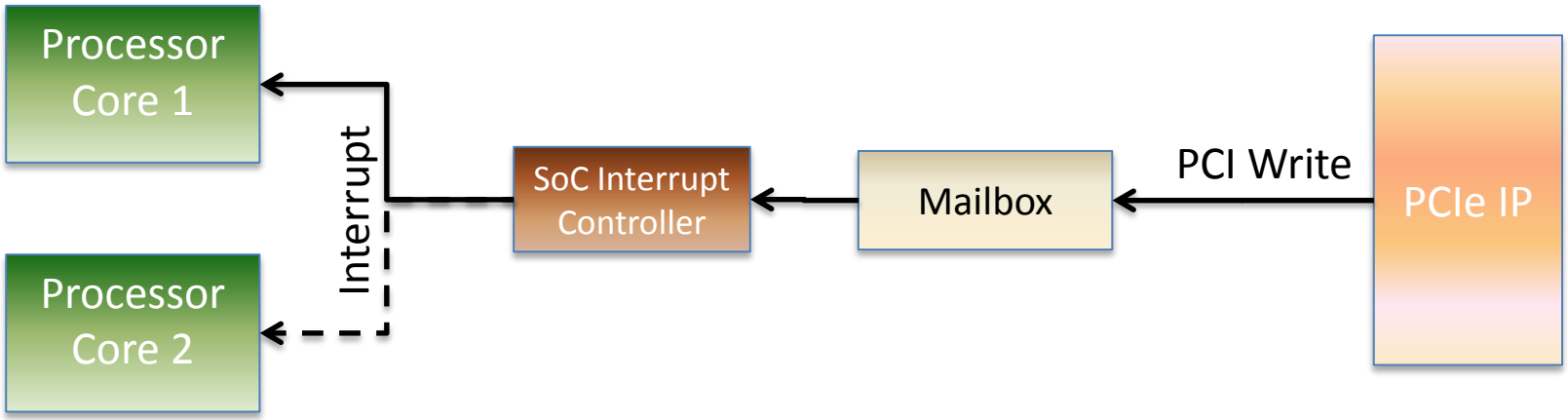
Payload Size: Implementation

- **Packet payload size vs Throughput**



Interrupts: Implementation

- **PCI protocol supports EP→RC interrupts**
- **Automotive co-processor systems often require RC→EP interrupts**
  - Must use memory-mapped SoC-level messaging/interrupts (ex. Mailbox)



PCI Express Functional Safety

Functional Safety

- **Automotive SoCs must comply to Functional Safety requirement for the target applications**

- **ISO 26262 defines Functional Safety for Automotive**
  - Defines four Automotive Safety Integrity Levels
  - (Least Stringent) **ASIL A, ASIL B, ASIL C, ASIL D** (Most Stringent)

- **Typical ASIL levels**
  - ASIL B for Infotainment (ex. Cluster warning lights)
  - ASIL C (Safety Island) for ADAS (ex. camera / radar)

Functional Safety: PCIe IP

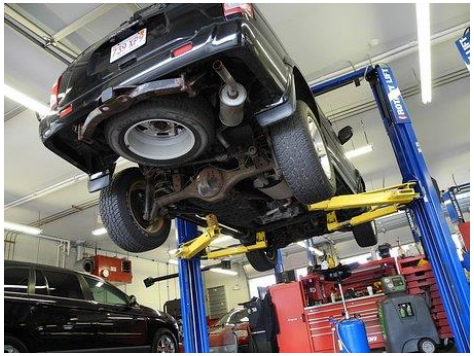
- **PCIe IP Functional Safety Requirements**
  - IP should be developed as a Safety Element out of Context (SEooC)
  - Must meet ASIL level defined by the SoC/application
  - Should come with Failure Mode, Effect and Diagnostics Analysis (FMEDA) report

- **Safety Features**
  - Data Path Protection via Parity
  - ECC protection on the RAMs
  - Configuration register protection
  - Debug and statistics capabilities
  - Safe operating mode

PCI Express Validation and Documentation

Electrical Validation

- **Automotive applications require**
  - Low DPPM (Defective Parts per Million)



  - Wide temperature range

Electrical PVT Validation

- **Process**
  - Must cover extreme Weak corner to extreme Strong corner of silicon manufacturing variation
  - Requires split-lot units and socketed (or multiple) validation PCB
- **Voltage**
  - Must cover Core and IO/Analog Voltage variation (e.g.. +/-5%)
  - Must check performance / trimming on internal LDOs
- **Temperature**
  - Automotive ambient temperature standard of -40 to 85C roughly translates to -40C to 125C at silicon junction
  - Must use on-die thermal diodes to measure temperature
  - Must deal with ice build-up and thermal shut-down

Test Equipment

- **Expensive Scopes and BERTs (100s of $Ks) are required for PCI Express TX and RX electrical validation**
- **Must remember to run instrument auto-calibrations per the recommended schedule**
- **Defective/Uncalibrated instruments can introduce unwanted noise into sensitive jitter tolerance testing**
  - Calibration expiring during validation can impact schedule
- **High-quality, phase-matched cables are needed**
  - See PCI-SIG recommendations
- **Must apply proper SMA connector torque**

Electrical Validation Automation

- **Comprehensive PVT testing requires many validation runs to cover all combinations**
  - Automation can make the validation less labor intensive

- **Automation tools:**
  - Robotic swapping of units (ideal, but not always practical)
  - SERDES Switch to change port/lane under test
  - Thermal chamber or Forced Air machine to vary Temperature
  - Programmable bench supplies to control Voltages
  - Sig-Test scripting to batch process TX waveforms
  - Automation software (e.g.. LabView) to tie it all together

Electrical Validation Automation

- **Example SigTest Python script**

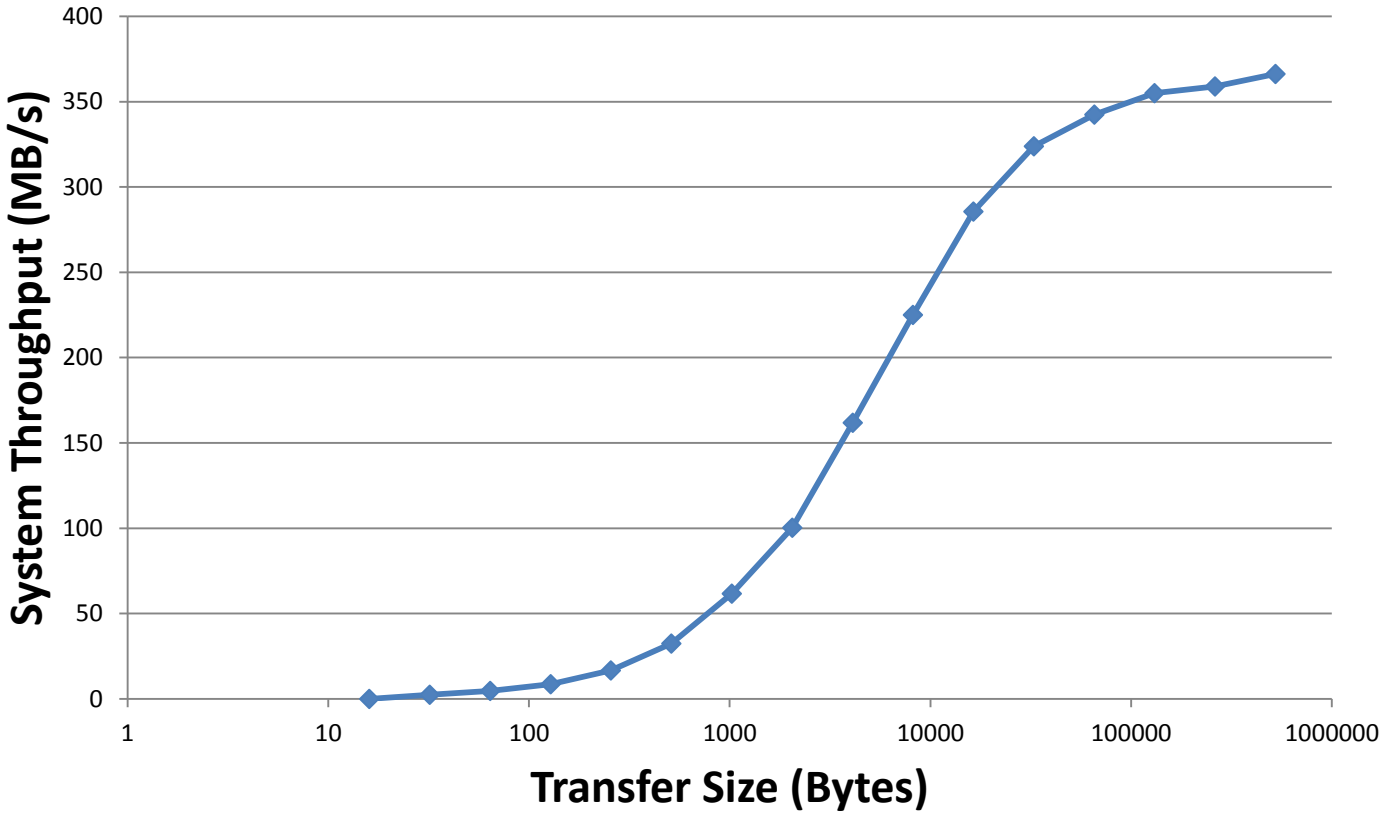
```
# File: SigTest.py

print "Running SigTest"
clock_waveform = "Lane0_5G_6dB_clock.wfm"
data_waveform = "Lane0_5G_6dB_data.wfm"
result_filename = "Lane0_5G_6dB_results.txt"
template = "PCIE_2_0_SYS\DUAL_PORT_SYS_CON_250.dat"

from subprocess import call
call(['SigTest', '/d', 'C:\pcietest', '/s', data_waveform, '/cs', clock_waveform, '/t',
template, '/o', result_filename])
```

Customer Documentation

- **Electrical / Timing Tables**
  - Typically reference the PCI Express Specification without reproducing
- **User Guide**
  - Based on IP vendor user guide, filtered to match Device integration
  - Adds clocking, reset, power, interrupt, and memory map details
  - Provides initialization steps
  - Describes required PHY programming
- **Errata**
  - Most PCI errata will come from IP vendor
  - Must filter/translate IP vendor errata to Device errata
    - Filter by Integration details and supported Device use cases
    - Workarounds must be evaluated for system feasibility
    - Not all IP errata will apply to the Device

Customer Documentation

- **Throughput measurements (ex. DMA writes)**



Customer Documentation

- **Layout guidelines to guide less experienced designers in SERDES routing best practices**

Table 8-25. PCIe PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within PCIe routing region	-	-	0	Cuts
Number of layers between PCIe routing area and reference plane (1)	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

Table 8-26. PCI-E Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCIe signal trace length			4700(1)	Mills
Differential pair trace matching			5(2)	Mils
Number of stubs allowed on PCIe traces(3)			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Pad size of vias on PCIe trace			25(4)	Mils
Hole size of vias on PCIe trace			14	Mils
Number of vias on each PCIe trace			0	Vias
PCIe differential pair to any other trace spacing	2×DS(5)			

Appendix

Reset: Implementation

PCIe IP Reset

PCIe IP Reset	SoC Resets	SoC Does Not Reset
Root Complex Mode	• SoC Reset causes PCIe IP Reset and EP Reset • SoC reinitializes PCIe IP and EP	• SoC stops PCIe transactions • SoC disables/resets EP • SoC issues PCIe IP Reset • SoC reinitializes PCIe IP and EP
End Point Mode	• RC asserts SoC Reset • SoC Reset causes PCIe IP Reset • RC does not Reset • SoC reinitializes PCIe IP • RC reinitializes PCIe IP	• RC issues Reset to PCIe IP • PCIe IP completes transactions • PCIe IP interrupts SoC • SoC issues PCIe IP Reset • SoC reinitializes PCIe IP • RC reinitializes PCIe IP

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